60V N-Ch Power MOSFET

V_{DS}		60	V
$R_{DS(on),typ}$	V_{GS}=10V	3.8	m
$R_{DS(on),typ}$	V_{GS}=4.5V	4.8	m
I_D		21	A

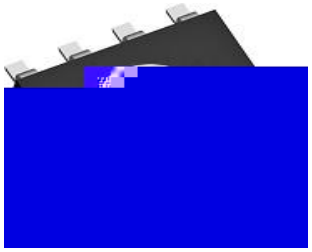
Feature

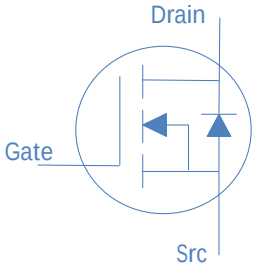
- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

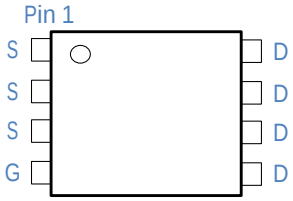
- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

SOIC-8





Part Number	Package	Marking
HGS048N06SL	SOIC-8	GS048N06SL



Absolute Maximum Ratings at T_j

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C	21	A
		T_C	13	
Drain to Source Voltage	V_{DS}	-	60	V
Gate to Source Voltage	V_{GS}	-	20	V
Pulsed Drain Current	I_{DM}	-	140	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C	240	mJ
Power Dissipation	P_D	T_C	3.1	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Lead	R_{JL}	23	
	R_{JA}	40	
Thermal Resistance Junction-Ambient (steady state)		75	

Electrical Characteristics at T_j

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1	1.8	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=60V, T_j	-	-	1	A
		V_{GS}=0V, V_{DS}=60V, T_j	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS} $_{DS}$=0V	-	-		
	g_{fs}	V_{DS}=5V, I_D=20A				
			-	3250		
Total Gate Charge	Q_g(10V)					

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

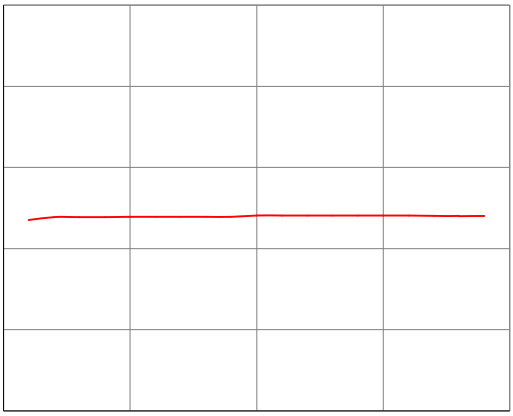
Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature
	

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

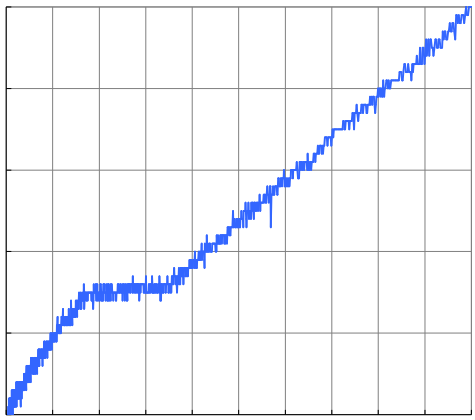


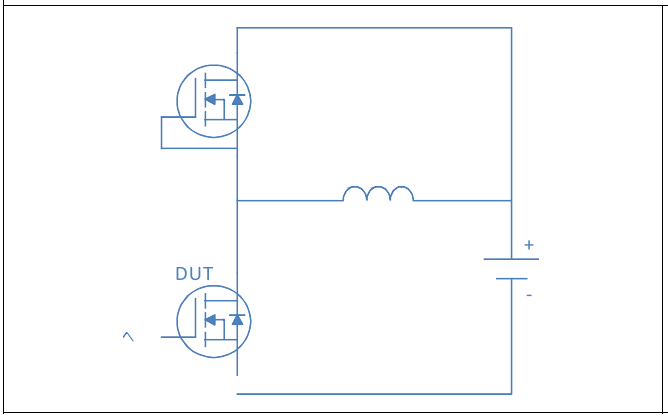
Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

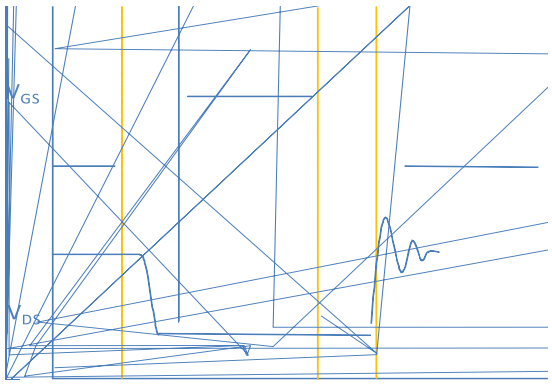
Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

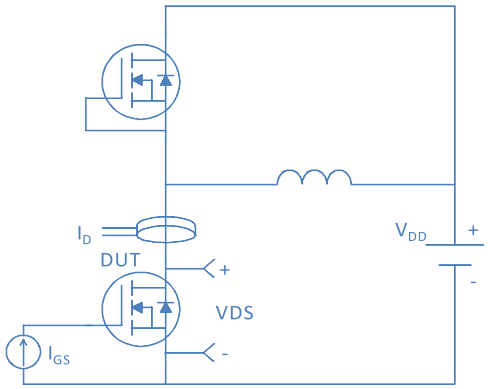
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

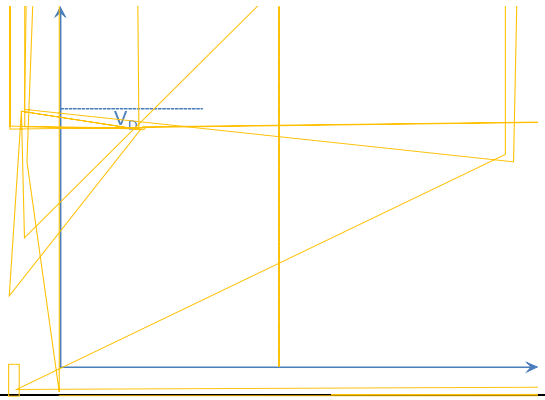
Inductive switching Test



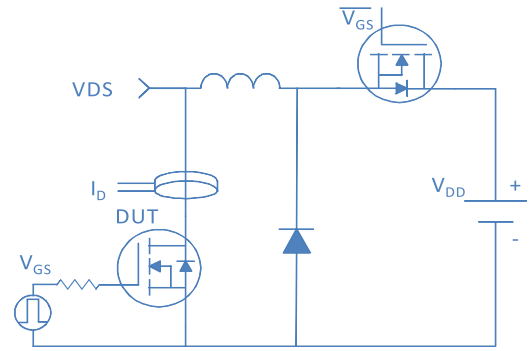


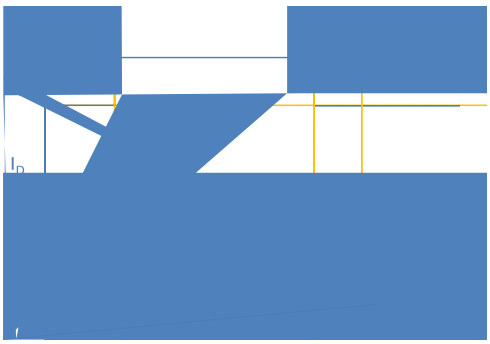
Gate Charge Test



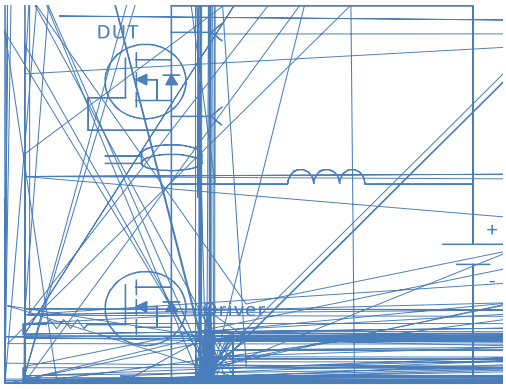


Uclamped Inductive Switching (UIS) Test



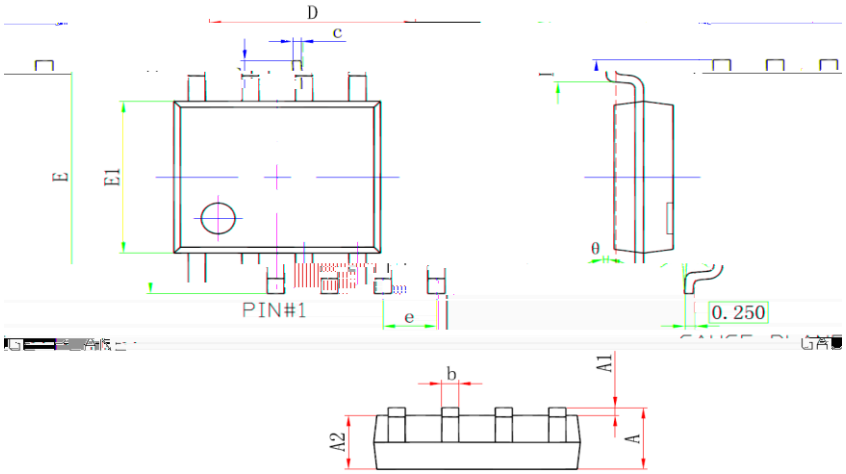


Diode Recovery Test



Package Outline

SOIC-8, 8 leads



In Inches			Dimensions In Millimeters		Dimensions
			0.100	0.250	0.004
			1.350	1.550	0.053
			0.330	0.510	0.013
1.270 (BSC)			0.050 (BSC)		
			0.150	0.157	
0.400		1.270	0.016	0.031	